ABSTRACT OF THE DISCLOSURE

A rate limiting circuit for data stream transmissions provides a generated clock signal to a buffer interposed between source and destination components so as to programmably adjust the maximum rate that data can be passed through the buffer. A counter is incremented by one each ($1+RL_{MAX}$) cycles of a clock signal, where RL_{MAX} is the larger of a user programmable value (RL) and a manufacturer one-time programmed value (SERL). A controller receiving a request to access the buffer for a read or write operation, checks the count of the counter before activating the access enable line. If the count is greater than zero, then the controller activates the access enable line while decrementing the counter by one. If the count is zero, however, then the controller waits until the count is greater than zero before activating the access enable line to grant the request.